Listing of Claims

1. (previously presented) A semiconductor device which integrates a plurality of semiconductor chips into a single package, comprising:

a first semiconductor chip which includes a plurality of first bonding pads outputting first signals having a first level; and

a second semiconductor chip which includes

a plurality of second bonding pads electrically coupled to a part of the plurality of first bonding pads to receive the first signals having the first level from the first semiconductor chip through the part of the plurality of first bonding pads,

a plurality of third bonding pads, and

a signal level conversion circuit,

wherein said signal level conversion circuit converts the first signals received through the plurality of second bonding pad into second signals having a second level different from the first level and outputs the second signals through the plurality of third bonding pads.

2. (original) The semiconductor device as defined in Claim 1, wherein the second level is greater than the first level.

Claims 3-9 (canceled).

10. (previously presented) A semiconductor device which integrates a plurality of

semiconductor chips into a single package, comprising:

a first semiconductor chip which outputs one or more first signals having a first level; and

a second semiconductor chip which includes a signal level conversion circuit,

wherein said signal level conversion circuit converts the first signals from the first semiconductor chip into second signals having a second level different from the first level.

11. (previously presented) The semiconductor device as defined in Claim 10, wherein said signal level conversion circuit includes a buffer driven at the second level.

12. (previously presented) The semiconductor device as defined in Claim 11, wherein said buffer converts an input signal at the first level into an output signal at the second level.

13. (previously presented) The semiconductor device as defined in Claim 10, wherein said signal level conversion circuit includes an I/O interface circuit adapted for bi-directional data flow.

14. (previously presented) The semiconductor device as defined in Claim 13, wherein said I/O interface circuit includes one or more tri-state circuits.

15. (previously presented) The semiconductor device as defined in Claim 10, wherein the second level is greater than the first level.